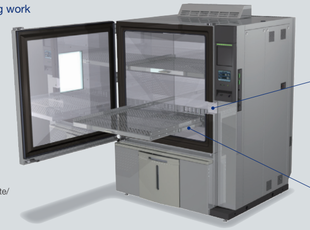
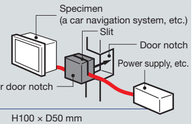
Available **Environmental Chamber** Modifications **for Semiconductor market**

Door Notch and Sliding Shelf

Applicable Series
Platinous J Series and AR Series

- Easy to install heavy objects
- Simplified wiring work





Door notch

Dimensions:	H100 × D50 mm

* Including dedicated rubber plug

Sliding shelf

Load capacity:	Maximum load capacity 100kg
Slide length:	Approx. 700 mm

https://espec.satori.site/products/catalog/usability#sec2

Slide Door

Applicable Series
Bench-Top Type Temperature (& Humidity) Chamber

- Simplified wiring work
- Sample demonstration available

Flat cable port type

Sample holder type

https://espec.satori.site/products/catalog/usability#sec6

Rectangular Cable Port

Applicable Series
Thermal Shock Chamber TSA Series

Simplified wiring for large connectors

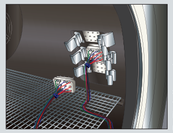
Dimensions:	H125 × D65 mm
Max. number of ports:	Maximum 2 on left side wall Maximum 1 on right side wall

https://espec.satori.site/products/catalog/usability#sec4

Removable Terminal Blocks　Sliding Panel-Mounted Terminal Blocks

Applicable Series
HAST Chamber

Simple wiring + simple installation = reduced work time



Terminal block allows 12-pin specimen signal terminals in the test area to be inserted and removed at once

Terminal block that slides to the front

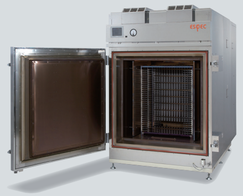
https://www.espec.co.jp/products/book/hast/#target/page_no=13

Semiconductor Heat Treatment System

Anaerobic Clean Oven (Oxygen concentration at 10 ppm)

Applicable Equipment
Anaerobic Clean Oven

- Ideal for low oxygen annealing required for 3D semiconductor packaging and integration.
- Supports heat treatment at oxygen concentrations as low as 10 ppm (0.001%) with Class 5 cleanliness
- Enables high-temperature annealing from 350 to 500 °C under low-oxygen conditions, with reduced process times through water cooling.



https://espec.satori.site/products/catalog/highperformance#sec7

Large-Capacity Types

• Large Highly Accelerated Stress Test System—HAST Chamber

Dimensions inside test area	Ø548 mm × L560 mm

https://www.espec.co.jp/products/env-test/ehs431/

Rapid-Rate Thermal Cycle Chamber

Internal dimensions (mm)	W800 × H500 × D750

https://www.espec.co.jp/products/catalog/tcc301.pdf

Power Semiconductor-Related Equipment

High Temperature Reverse Bias Test System

Applicable Series
HTRB HTGB H3TRB AMI

When the voltage of a power device is switched off, inductors in the circuit can generate surge voltages that may damage the device. Reverse bias testing is repeated to evaluate and improve product reliability.

Drain power supply	0 to 2 kV or 0 to 3 kV
Gate power supply	0 to ±30 V or 0 to ±35 V
Temperature control	In-chamber DUT board connection type: 200°C or 350°C

* Temperature/humidity type is also available.

https://www.espec.co.jp/products/measure-semicon/bias/

Power Cycle Test System

Applicable Series
RBS-PST

On/off current cycling in power devices causes self-heating, which can lead to wiring disconnections and damage to heat dissipation circuits. Power cycle testing evaluates these effects to improve product reliability.

Major test modes

Continuous mode	Controls cooling water temperature and volume to maintain the device at the set temperature while "Ice" remains constant.
Vf cycle mode	Cycles "Ice" on/off to achieve and maintain the target specimen temperature.
Cycle mode	Cycles "Ice" on/off at timed intervals

https://www.espec.co.jp/products/measure-semicon/iet-igbt/

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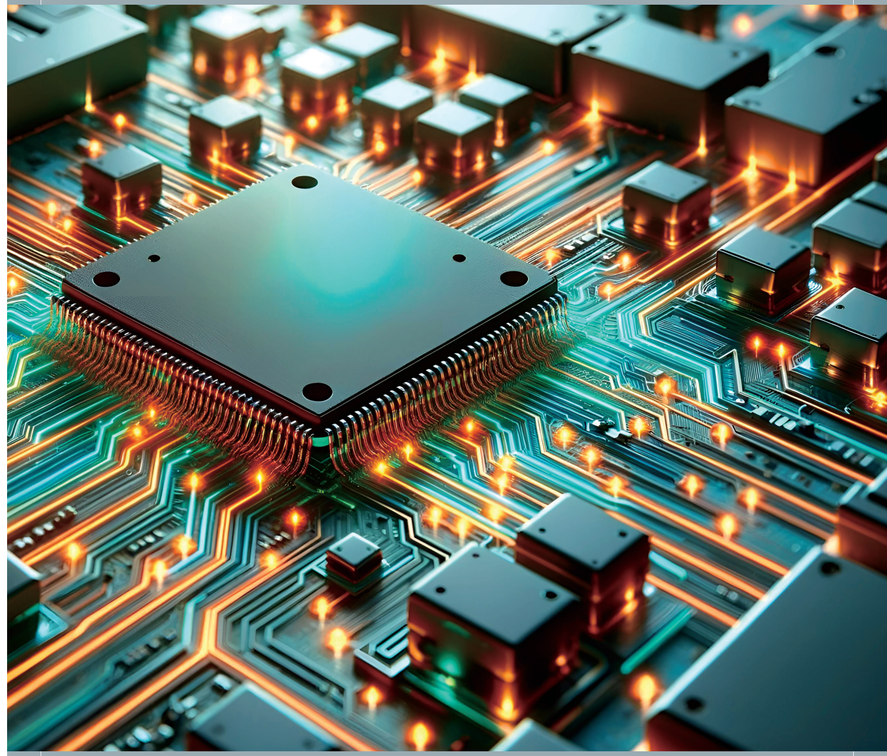
Quality is more than a word

ESPEC

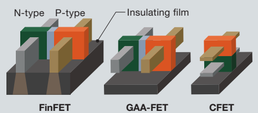
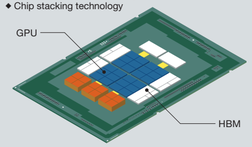
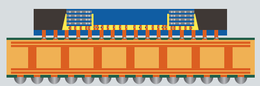
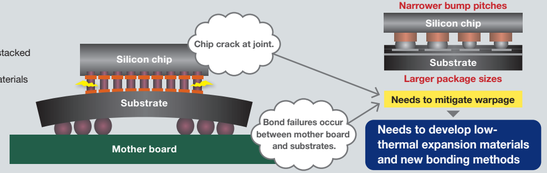
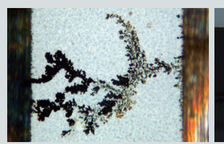
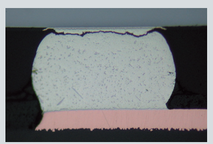
SEMICONDUCTOR RELATED EQUIPMENT



Thermal management is critical to the future of semiconductors.

Semiconductor-Related Test Equipment/System Lineup

As semiconductor performance and integration continue to advance, managing heat has become one of the most critical challenges. Effective thermal solutions are essential for enhancing performance, ensuring reliability, and extending device lifetimes. ESPEC offers a comprehensive lineup of systems designed with a focus on thermal management to support reliable heat control.

Process	Front-end process	Back-end process	Inspection	Reliability test field							
Technology trends	Development of leading-edge processes of 2 nm level.	Heterogeneous (chiplet) technology	Screening during the process, final inspection	Temperature and humidity test, thermal cycle test	Highly accelerated test (PCT)	Electrochemical migration evaluation of microscopic pattern insulation (HBT/HHBT)	Thermal cycle test, Rapid temperature change	Thermal shock test	Evaluation of microcracks in wire joints Reliability testing of microscopic wiring connections	HALT / HASS	Thermal management
	◆ EUV lithography ◆ Advanced deposition and lamination ◆ High-layer-count etching ◆ Micropattern (fine-pattern) cleaning ◆ Automated technology 	◆ Leading-edge 2.xD and 3D packages ◆ Large interposers ◆ Chip stacking technology ◆ Fine redistribution layers ◆ Optoelectronic integration technology ◆ Low-dielectric materials 	◆ Inspection methods for leading-edge processes such as the 2 nm node ◆ Inspection methods for chip stacking technologies ◆ Inspection methods for chiplet integration processes	◆ Compliant with reliability standards for leading-edge processes ◆ Enables reliable lifespan prediction for microscopic wiring processes ◆ Compliant with reliability standards for advanced 3D packages ◆ Enables reliable lifespan prediction for microscopic packaging technologies							
Quality trends	Issues of leading-edge process operations, quality evaluation at the wafer level	Quality evaluation in the middle-end and back-end process	Extraction rate improvement for leading-edge devices	Allowable high heat load, microscopic bonding technologies, and technologies to mount more pins							
	◆ Reliability of chip bonding materials such as CoW ◆ Quality assurance methods in the front-end process 	◆ Fine redistribution layers and TSV interconnections ◆ Impact of local chip heat generation ◆ Quality of microscopic processes in the middle-end stage 	◆ Process inspection in the front-end stage ◆ Process inspection in the middle-end stage ◆ Process inspection in the back-end stage ◆ Burn-in test for high-value semiconductors	◆ Reliability of TSV joints ◆ Countermeasures for localized chip heat generation ◆ Board-level heat dissipation design ◆ Mitigation of thermal expansion between stacked materials ◆ Evaluation of multiple types of bonding materials 			 Phenomenon of electrochemical migration (Ion migration)  Microcracks at a joint	◆ Compliance with semiconductor test standards JEITA ED4701/001A JEITA ED4701/100A Test method 102A: High-temperature, high-humidity bias test Test method 103A: High-temperature, high-humidity storage test Test method 104A: Humidification + Packaging stress series test Test method 105A: Thermal cycle test JEITA ED4701/200A Test method 201A: High-temperature storage test Test method 202A: Low-temperature storage test (reference test) Test method 203A: Temperature and humidity cycle test (reference test)	
Our recommended products	Wafer-level semiconductor characterization equipment	High-performance, Anaerobic Clean Oven	Package level semiconductor characterization equipment	Burn-in test-related equipment	Temperature and humidity chambers	HAST chamber	Semiconductor measurement systems	Rapid-rate thermal cycle chamber	Thermal shock chamber	Semiconductor measurement systems	HALT / HASS	One-device, spot heating and cooling
					Recommended system for reliability evaluation testing: Electro-Chemical Migration Evaluation System (AMI Series)			Recommended system for reliability evaluation testing: Conductor Resistance Evaluation System (AMR Series)				
	◆ Semiconductor Parametric test system (Wafer-Level) AMM Series ◆ TDDB Evaluation System (Wafer-Level) AMM Series  https://www.espec.co.jp/products/catalog/spa.pdf	◆ SCO Series ◆ PVHC Series  https://www.espec.co.jp/products/env-test/sco/	◆ Semiconductor Parametric test system (Package-Level) AMM Series ◆ TDDB Evaluation System SMU Type (Package-Level) AMM Series  https://www.espec.co.jp/products/catalog/spa.pdf	◆ Static Burn-In System Dynamic Burn-In System  https://www.espec.co.jp/products/catalog/rbs.pdf	◆ Platinous Series ◆ AR Series  https://www.espec.co.jp/products/book/ar01/#target/page_no=1 Temperature and humidity chamber lineup https://www.espec.co.jp/products/catalog/temp_chamber_lineup.pdf	◆ EHS Series  https://www.espec.co.jp/products/catalog/hast.pdf	◆ Bectrochemical Migration Evaluation System (AMI Series)  https://www.espec.co.jp/products/catalog/ami.pdf	◆ TCC Series  https://www.espec.co.jp/products/catalog/tcc151.pdf	◆ TSA Series ◆ TSD Series ◆ TSB Series  https://www.espec.co.jp/products/catalog/tsa.pdf	◆ Conductor Resistance Evaluation System (AMR Series)  https://www.espec.co.jp/products/catalog/amr.pdf ◆ Electro-Migration Evaluation System (AEM Series)  https://www.espec.co.jp/products/catalog/aem.pdf	◆ T-Series  https://www.espec.co.jp/products/book/halt_hass/#target/page_no=1	◆ MTA Series  https://www.espec.co.jp/products/catalog/mta.pdf
	Defects in the front-end process can be evaluated at the wafer level using a combination of critical parameter tests, supported by a fully automated prober, to ensure reliability.	An ultra-low oxygen atmosphere enables polyimide imidization at high temperatures (400 °C and above) while protecting devices from thermal degradation. Heat treatment with precise temperature uniformity ensures the formation of consistent insulating films.	Semiconductor characteristics can be evaluated at the package level to assess the reliability impact of devices assembled or packaged during the back-end process. Using a temperature chamber, transistor characteristics can also be measured in real time under controlled temperature conditions.	Burn-in testing is used to screen high-performance semiconductors such as SoCs and GPUs for potential defects. Devices are subjected to voltage loads or input signals at elevated temperatures to identify and eliminate failures before shipment. This all-in-one system integrates burn-in functionality with a temperature chamber, providing a complete testing solution that has been widely adopted by customers.	Our chambers perform temperature and humidity testing in compliance with semiconductor reliability standards. A wide range of models are available, offering different capacities and environmental ranges to meet specific testing needs	This series of dedicated PCT and HAST chambers accelerates deterioration in the form of failure mechanisms by applying pressure and humidity during semiconductor reliability testing.	This evaluation system provides real-time detection of insulation failures, such as electrochemical migration, in wiring patterns on RDLs and substrates. When paired with a temperature and humidity chamber, its dedicated measurement circuits enable high-speed, high-accuracy capture of instantaneous insulation failures.	This chamber applies rapid temperature changes to specimens in full compliance with JEDEC standard testing and screening requirements. It is ideal for evaluating automotive semiconductors, sensors, and other electronic devices.	Thermal shock chambers are designed for reliability testing by accelerating deterioration mechanisms, such as joint cracking, through rapid cycling between high and low temperatures. Both elevator-type and liquid-to-liquid configurations are available.	Microcracks in joints and other connection defects can lead to conduction failures under rapid temperature changes. When integrated with a thermal shock chamber, the conductor resistance evaluation system measures resistance in real time within a controlled temperature environment, enabling fast and accurate assessment of connection reliability.	This dedicated system evaluates electromigration in microscopic wiring. It supports accelerated testing at temperatures up to 450 °C.	Performing HALT (Highly Accelerated Life Testing) early in product development helps uncover design weaknesses, significantly improving reliability. These systems also support HASS (Highly Accelerated Stress Screening) for production-level screening.	The spot cooling and heating system is chamber-free, directing heated or cooled air through a hose to the specimen. With a front heater capable of changing air temperature at 100 °C/min, it enables significant reductions in testing time.
Standard	–	–	–	–	ED-4701/100A, 103A, IEC60068-2-1, IEC60682-2	IEC60068-2-66, ED-4701/100A JESD22A118B	–	IEC60749-25 JESD22-A104F, ED-2531BNa	MIL-STD-883L, IEC60068-2-14Na, ED-2531BNa	–	–	–