

Highly Accelerated Life Test (HALT) Program at Space Systems Loral

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ABSTRACT

Highly Accelerated Life Testing (HALT) is used in the commercial electronics industry to improve product robustness prior to starting production. The basic theory is that testing well beyond expected, intended-use environments may uncover design flaws that could become field failures after a product is in production. By fixing issues prior to starting production, costly recalls can be avoided. HALT has proven to be effective, as evidenced by its wide incorporation in the commercial electronics industry. Could HALT also be worth the time and expense of performing on commercial satellite hardware, which is designed to rigorous standards and tested over military-grade environmental test specifications? This paper summarizes Space Systems/Loral's (SS/L) initial experience with HALT, experience over time, and refinement of the traditional HALT process with emphasis on finding the operating limit margins before purposely searching for any failure limits. The methodology used by SS/L has proven to be effective when introducing new technologies and complex designs for use on commercial satellites.

KEY WORDS

Highly Accelerated Life Test (HALT), Commercial satellites, MIL-STD-1540, Qualification

INTRODUCTION

The suppliers of most U.S. commercial satellites qualify hardware to tailored versions of Mil-STD-1540E and, for European suppliers, ECSS-E-10-03A, which has similar qualification test margins and environmental requirements. The philosophy behind both of these documents is to test units to predefined margins over flight predictions, for launch vibration and on-orbit thermal excursions, for example. This approach has served Space Systems/Loral (SS/L) well, as evidenced by excellent performance in the first year of operation, the time period monitored for robustness against infant mortality issues. Occasional qualification and acceptance test program escapes, however, adversely affect cost and schedule prior to launch. In this highly competitive market it is important to drive the number of failures after unit-level qualification as low as possible, with an ultimate goal of zero. The occasional qualification and acceptance test programs escapes are at least partially due to the fact that testing to flight predictions with some amount of margin does not fully protect against the statistical nature of design and manufacturing tolerances or of combinations of statistical variations. Figure 1 shows that high and low "tails" of normal stress and strength distribution curves can overlap to produce an area of unreliability where failures can occur for any flight hardware unit type over its production life cycle.

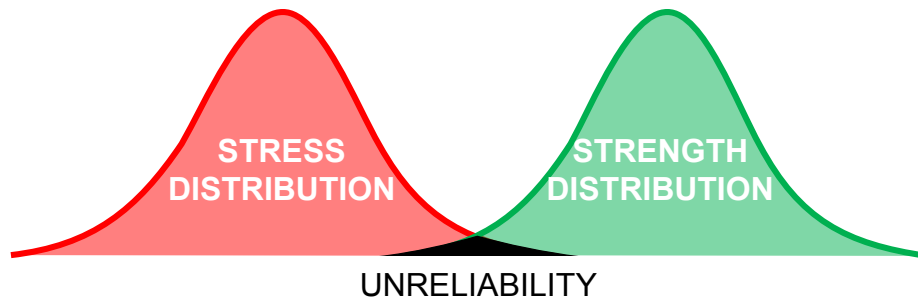


Figure 1: Statistical Nature of Stress vs. Strength [ref: From: Reliability Growth Management in non-Military Industry, by Clifton J. Seusy Hewlett-Packard Company Disc Memory Division, Boise, Idaho]

Another way to state this point is that even if a unit passes 1540E or E-10-03A qualification, the margin remaining to failure is not known. The unit may be close to a limit that might not manifest itself in a failure until several production units are built and tested. Probabilities of not finding issues during qualification and acceptance temperature testing are illustrated in Figure 2.

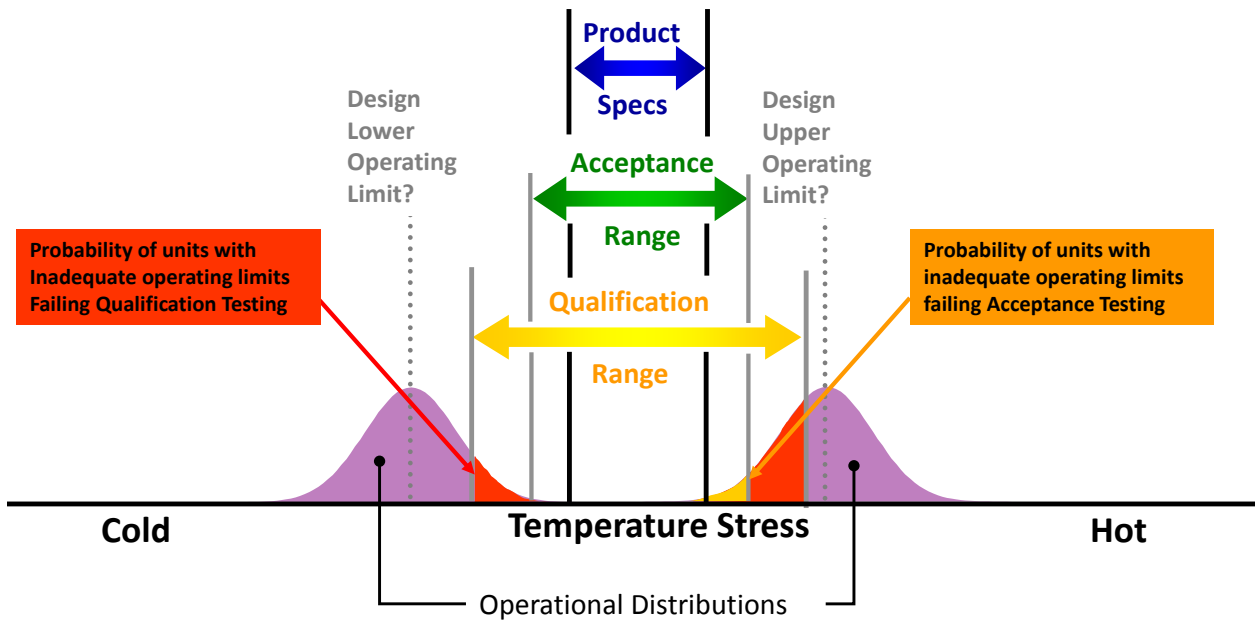


Figure 2: Probabilities of not finding issues during qualification and acceptance temperature testing

Finding issues on the ground prior to launch can be painful from the satellite manufacturer's cost and schedule standpoint. However, finding an issue on orbit is far worse. It can severely damage a customer's business plan, result in the loss of a manufacturer's on-orbit incentive revenue, and damage a manufacturer's reputation throughout the industry.

Since new technologies are frequently introduced to meet growing commercial satellite customer demands for power, bandwidth, pointing, etc., effective qualification test programs are essential. To reduce the number of design issues found in production after completion of MIL-STD-1540E qualifications and to reduce the probability of on-orbit failures, SS/L started performing Highly Accelerated Life Testing (HALT) on new development units in 1999. The next section provides

a basic introduction to HALT to set the context for the following sections, which cover SS/L's HALT program introduction, experiences, and results. This paper provides only limited detail of the history and theory of HALT, since many references for HALT can be found online. Appendix 1 lists HALT definitions from a number of different references. Additional information is available under the "resource" tab at

http://www.opsalacarte.com/Pages/resources/resources_techpapers.htm#haltandhass.

HALT HISTORY, BASIC THEORY, AND APPLICATION

HALT involves the accelerated application of environmental and operational stresses to levels significantly above the design specifications of a unit. The intent of these higher stresses is to stimulate failure modes and mechanisms. Note in Figure 3 that by increasing the applied stress level, the amount of unreliability available to detect (the overlapping area of the two curves) is increased compared to that shown in Figure 1.

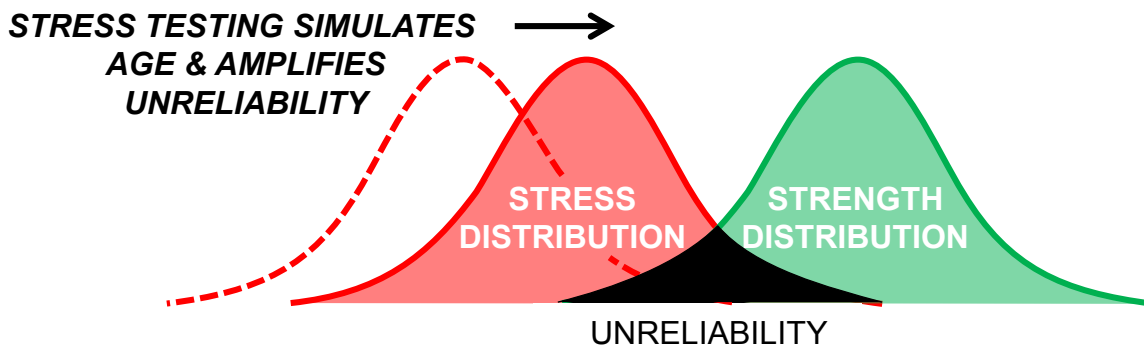


Figure 3: Stress Testing Principle [ref: From: Reliability Growth Management in Non-Military Industry, by Clifton J. Seusy Hewlett-Packard Company Disc Memory Division, Boise, Idaho]

The question that many people ask when introduced to the HALT concept is whether HALT precipitates failures that will not occur in fielded units that operate in more benign and expected environments compared to the HALT stimulus. While this may sometimes be the case, the authors believe that in most cases HALT does identify real issues that can occur statistically over time. Numerous HALT papers published on commercial electronics indicate that failures induced in this manner accurately predict the failure modes that the product will encounter over time. One possible explanation for this, beyond pure stress versus strength statistics, is that strength decreases with age. Note in Figure 4 that the shifting of the strength statistical distribution to the left over time results in a similar amount of increased unreliability available to detect (the overlapping area of the two curves) as was previously shown in Figure 3, i.e., increasing test stresses and decreasing strength over time can produce similar results.

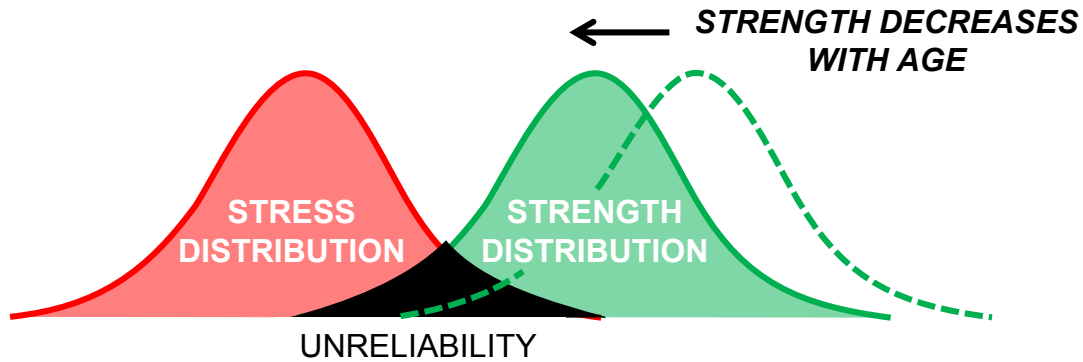


Figure 4: Effect of Time on Strength [ref: From: Reliability Growth Management in Non-Military Industry, by Clifton J. Seusy Hewlett-Packard Company Disc Memory Division, Boise, Idaho]

Thus the title “Highly Accelerated Life Test” indicates that time to failure is “accelerated” by increasing the test stress levels. As an example of how Figures 3 and 4 are applicable to the commercial satellite business, consider that it is typical for low-level assemblies to be vibration tested, then tested again at one or more higher levels of assembly. Each successive test adds some amount of cumulative fatigue stress, and then the unit must also survive the stresses induced by the launch prior to it performing its primary mission on orbit. The cumulative amount of vibration stress demonstrated in SS/L’s HALT program is beyond what any unit will be subjected to during unit acceptance test and any subsequent stresses induced at higher levels of integration testing and launch.

By determining the root cause for each failure mode stimulated by HALT and implementing design changes to prevent their recurrence, product robustness, and thereby reliability, is improved. In other words, a successful HALT program will quickly create realistic equipment failures from which the designer learns root cause, potentially implements corrective action, and optimizes the design to push product limits out as far as possible. The fundamental differences in philosophy between MIL-spec qualification testing and HALT can be described as follows:

It may be typical for companies to hope that a unit passes the MIL-spec qualification test, or to explain away a failure, if one does occur, as an anomaly not to worry about. With HALT, however, the goal is to try to force failures to understand product margins and identify weak links in the design in order to fix them and make the product more robust prior to moving into production.

Improved product robustness after HALT is illustrated in Figure 5.

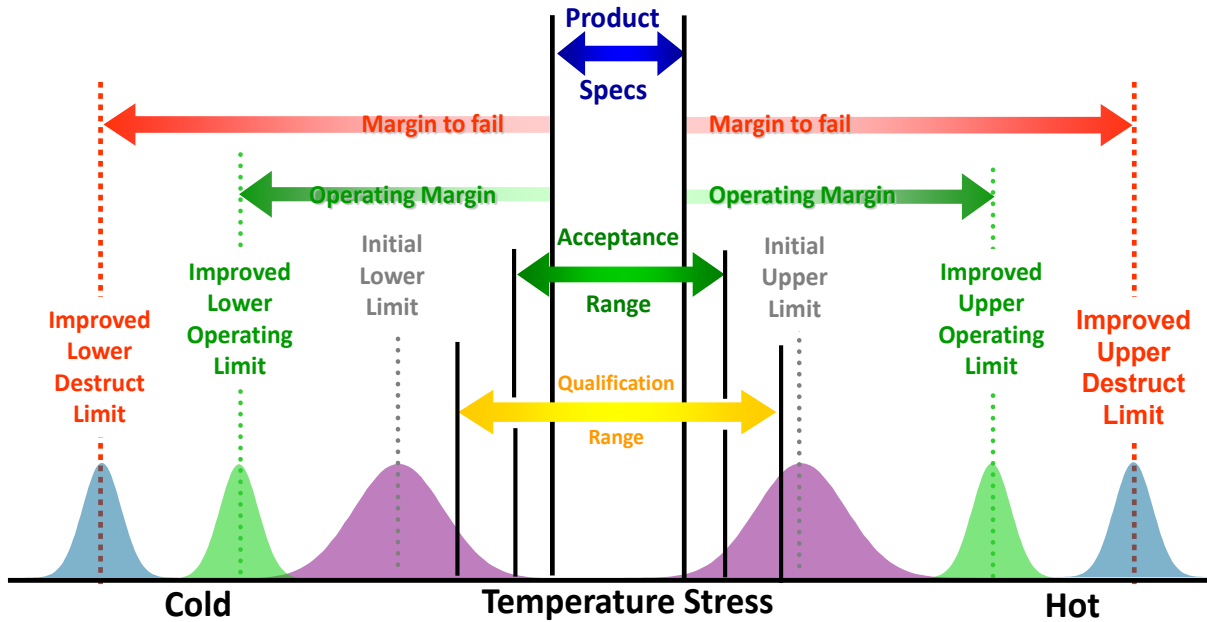


Figure 5: Improved product robustness after HALT [ref: Adapted from: HALT, HASS and HASA Explained, by Harry W. McLean American Society for Quality, Quality Press, Milwaukee 53203, Published 2009]

Stresses applied during HALT at SS/L typically include thermal limits (hot and cold), thermal cycling (rapid rate transitions), random vibration, and combined thermal cycling with random vibration. Depending on the particular unit, electrical or other mechanical stresses can be applicable (voltage, frequency, current, RF or DC power, relay switching, tensile load, etc.). During the HALT process, operational limits and destruct limits of a unit are determined:

- Operational limits: unit does not meet a performance parameter at some stimulus level but comes back into specification after the stimulus level is reduced
- Destruct limits: unit ceases to function and does not resume normal operation until repairs are affected

The myth exists that fixing issues found during HALT unnecessarily adds significant cost, complexity, or mass to units. Testing at SS/L has shown otherwise. Significant gains in product margins can sometimes be realized by simple modifications such as changing a resistor value or improving a part attachment technique. Properly performed, HALT will increase the probability of successful first-pass qualification testing and reduce the probability that latent design errors will be found during the production phase.

INTRODUCTION OF HALT AT SS/L

Many companies, including Hewlett-Packard and Otis Elevator Company for example, reported significant savings after implementing HALT programs. Initially, SS/L did not believe the time and expense of HALT testing was relevant to satellite technology developed to strict aerospace design guidelines and qualified to industry standard environmental qualification specifications. It was only after a unit had passed qualification but we could not solve an elusive part problem in

flight production (explained further in the next section), that we first decided to use HALT. The success we had in solving this problem lead to the first traditional HALT on a DC/DC converter at SS/L. Over the next 16 years, SS/L's HALT program went from limited use to becoming an integral part of our new product development and qualification process. Table I gives a top-level chronological summary of key milestones in SS/L's HALT program.

Table 1: SS/L HALT Evolution

Date	Event / Hardware	Comments
November 1996	Power Control Unit (PCU)	Used to solve elusive part-level problem
January 1999	15W DC/DC converter	First unit-level HALT
May 2000	Stationary Plasma Thruster (SPT) Power Processing unit trays	First complex unit HALT (multiple electronic trays tested separately)
February 2002	Super Power Subsystem (SPS)	First use of HALT where deemed appropriate for an entire new subsystem
September 2008	RAD 750 processor tray	First HALT of a subcontracted unit
Current	All new hardware	Cross functional team determines at Design, Development and Qualification (DDQP) review if new or "stretched" technology warrants HALT

SS/L's First Use of HALT

SS/L won the Tempo program in 1993, which ultimately became a DIRECTV satellite, the first satellite with high enough power to make direct broadcast TV possible to all of the U.S. After we won this contract, several subsequent high-power satellite contracts were awarded, all of which were dependent on the successful qualification of a new Power Control Unit (PCU) needed for the 100V regulated power bus subsystem. Throughout the new technology development, we were plagued with yield problems with parts needed for the PCU. Even though we increased the part level screening tests, a few failed during PCU acceptance testing after the completion of part and PCU qualifications. Because the failure rate was low and the damage was always significant, failure analysis was difficult, and the root cause of the failures was elusive. All programs pressed on hoping that the PCU acceptance testing was a sufficient unit-level screen. After we had a few failures at the satellite level, however, we knew that we did not understand the problem and had to stand down all programs until we determined root cause and fixed the problem. With typical large satellite late fee penalties and several spacecraft under construction, this was a significant issue for SS/L and for our customer's business plans. To help solve this problem, we contracted an outside testing service to perform HALT testing on the parts. We were able to get them to fail consistently using HALT step stress testing, specifically voltage and temperature. With more failed samples, we were able to determine the root cause in a matter of a few days. The redesign was relatively simple, so we were able to get all the programs back on track in a short period of time. Thus, our first experience with HALT helped us solve a problem that we had been struggling with for many months, in a few days.

SS/L's First Development HALT

After the initial success with solving our part problem, SS/L made a capital investment for our own HALT chamber (Figure 6).



Figure 6: SS/L HALT Chamber

The first SS/L unit (implemented in a single tray) that underwent HALT during development was a 15W DC/DC converter that was designed to provide power to payload units. Since there could be a very high number of these units on any one satellite, it was important to find any design deficiencies before it passed qualification and was in production. We performed testing in the sequence shown in Figure 7.

Hybrid circuit “screening rejects” were used in the 15W converter in order to save money. One failure of a hybrid circuit occurred during rapid thermal cycling and two failed during vibration testing. Although we were not sure why they failed, we initially attributed all three of these failures to the fact that they were not controlled as flight parts after they were rejected during the electrical screening process. It was not until stacked capacitors completely dislodged from their mounting pads during combined environments HALT that we understood why the hybrids had been failing. Subsequent analysis proved that cracked lead attachments (see Figure 8) were causing intermittent open circuits that were overstressing the hybrids and causing them to fail electrically.

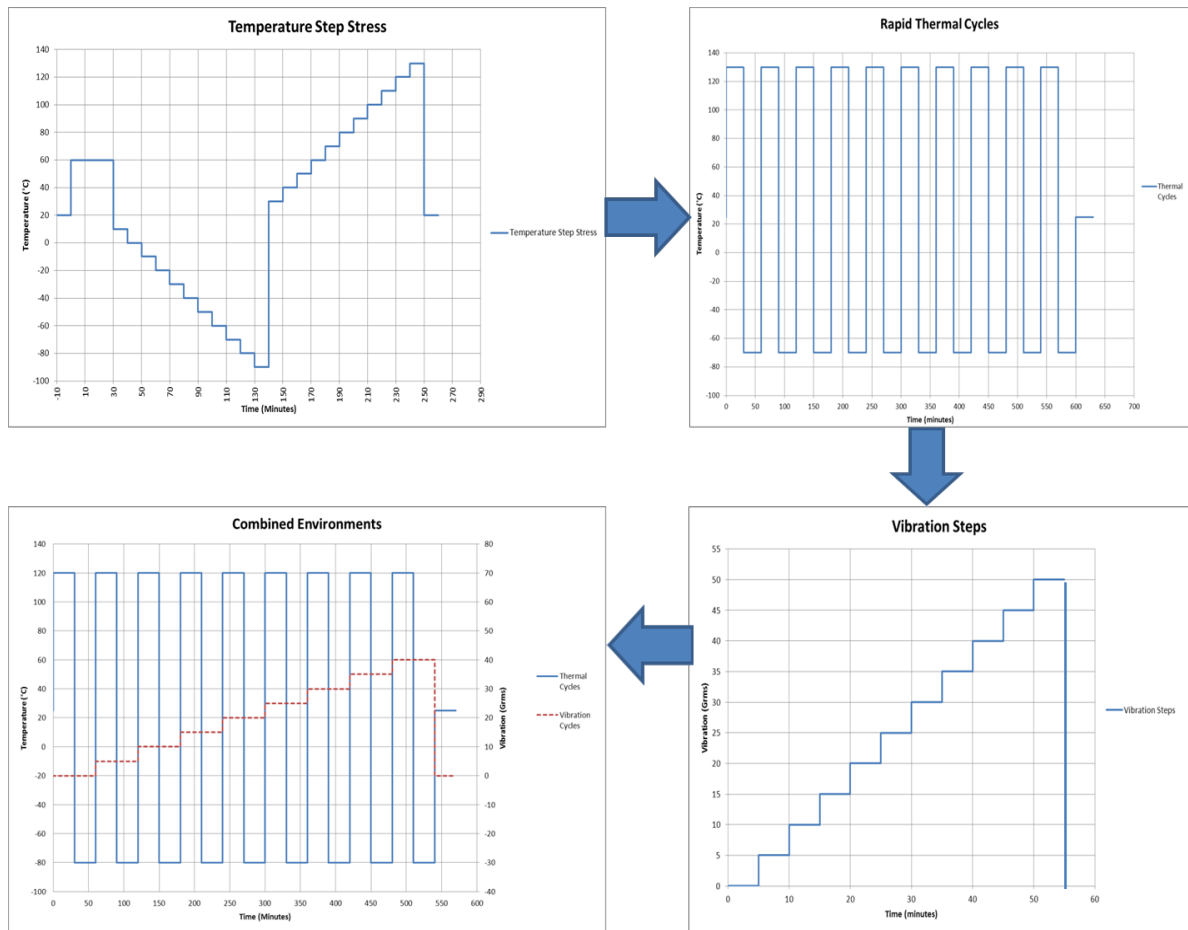


Figure 7: 15W DC/DC Converter HALT Environmental Test Sequence

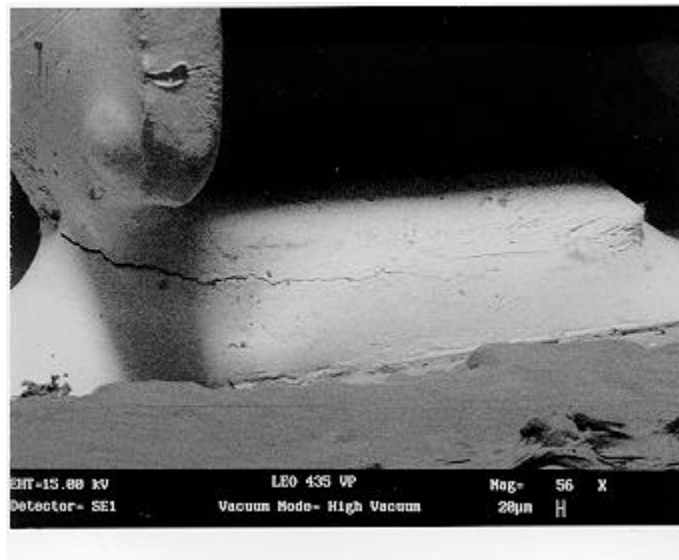


Figure 8: Cracked Capacitor Solder Joint

Thus testing beyond environmental requirements brought light to a manufacturing weakness that existed at the time the test article was manufactured. It was obvious only after the investigation that the pads were undersized for the mass of the parts.

One of the key challenges for any HALT campaign is to do it early enough that you can implement a design iteration if issues are uncovered that need to be fixed prior to starting traditional MIL-STD-1540 qualification and doing it late enough that it is representative of the qualification unit. For this reason we always have the HALT team ask the design and production team what nonflight features are present in the unit that will be tested. This information is used to jointly determine if the test article is mature enough to proceed with the HALT. The HALT on this 15W DC/DC converter also induced a failure on a nonflight attachment (see Figure 9) that had not been brought to the attention of the HALT team during the test readiness review prior to the beginning of HALT. This gave us even more confidence that HALT has the ability to detect nonrobust features of any product.



Description The inductor post (white arrow) fractured at the base, where it was soldered to the board.

Figure 9: Nonflight Manufacturing Process Detected by HALT

Finding these significant issues during our first tray-level test validated the value of HALT. Thus it justified expanding our HALT program to additional trays, more complicated units and, eventually, an entire subsystem as indicated in Table 1.

The next sections will discuss how HALT is integrated into new product development at SS/L today. Then we will show some sample results that validate the success of our HALT approach for testing commercial satellite equipment.

HALT PROCESS AT SS/L TODAY

a. Design, Development, and Qualification Plan

Units or components that use materials, technologies, manufacturing processes, packaging, or functionality that were not previously space qualified are classified as a Category A. The responsible engineer for any Category A units must create a Design,

Development, and Qualification Plan (DDQP) to identify high-risk aspects of the design and plan the testing and analyses necessary to mitigate them. The decision whether or not to perform HALT at SS/L is normally made during the integrated product team review of the DDQP.

b. Example Considerations to Determine if HALT will be Performed or not

This section provides an example of considerations that drove the decision to perform HALT on an Extended Enhanced Serial Interface Adapter Module (EESIAM) that was being developed for the SS/L command and control subsystem. Risk items identified during the DDQP review included the following:

- 4X capability growth over the heritage unit (See Figure 10)
- High component placement density
- Larger tray size than any previous flight-qualified unit
- New ASIC and new High Side Driver (and associated interactions with other flight heritage ASICs)
- Mission criticality and complexity

Any one of these factors probably would not have been significant enough to warrant the time and expense of HALT. The combined development risk of all of them together, however, justified using HALT on the EESIAM.

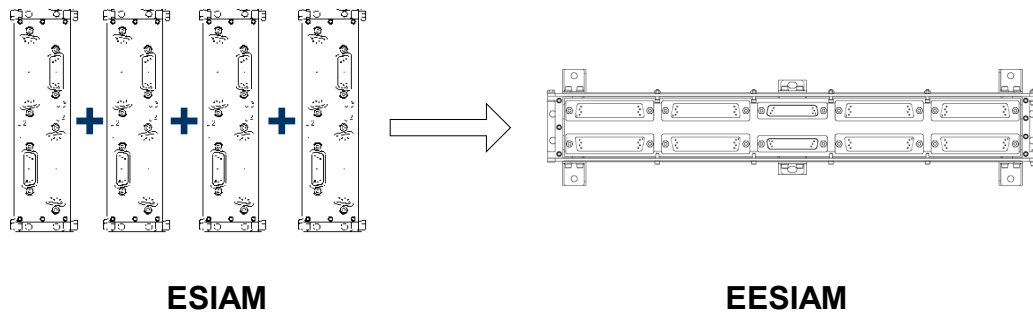


Figure 10: 4X capability growth from Heritage ESIAM to IR&D EESIAM unit

Because of the complexity of most modern satellite technology today, it is difficult, or perhaps impossible, to predict what new feature will cause problems during traditional qualification or possibly slip through and cause issues during production. In this case, we used a prototype High Side Driver (HSD) in order to perform the HALT early enough in the design process to be able to perform a design iteration of the EESIAM, if needed, and still make the qualification schedule. HALT detected one known issue in the HSD that was already scheduled to be fixed and one additional issue that was previously unknown. The early identification of the unknown issue resulted in significant savings, as we were able to make both fixes in one ASIC design iteration instead of two in series (if the second would have been detected in traditional qualification or subsequent acceptance testing that followed). In addition, another nonflight issue was found, further validating HALT's effectiveness in identifying nonrobust features.

SUPER POWER SUBSYSTEM (SPS) EXAMPLE

We have discussed SS/L's first HALT to help figure out the root cause of an elusive part problem, as well as our first HALT on a simple power converter and on a complex digital unit. In this section we discuss our first broad scale HALT campaign, in which a significant number of issues were discovered and resolved, and offer on-orbit performance results that conclusively show the robustness of the resulting products.

The first broad HALT campaign at SS/L was on our Super Power Subsystem (SPS), an upgrade to the LS1300 spacecraft power subsystem. By changing from nickel hydrogen to lithium ion (Li-ion) batteries and by making changes to our solar arrays, we were able to increase 15-year end-of-life power from 12 KW to 20 KW. A suite of power electronics was also needed to charge and discharge the Li-ion batteries, as well as control and distribute this increased amount of power. The DDQP process gave us specific risk identification information that was used to propose HALT on most of the power electronics trays. Since post qualification failures on any one of these trays would certainly cause significant cost and schedule impact to the first program, especially if detected at the satellite integration and test level, extra funding was allocated by management to perform HALT as indicated in Table 2.

For each of these trays, the following HALT was performed in the sequence indicated below and similar to the illustrations shown in Figure 7:

1. Temperature step stress (hot and cold)
2. Rapid temperature cycling
3. Vibration
4. Combined rapid temperature cycling with vibration

The most significant finding during the entire HALT campaign was during vibration testing. Since we were trying to get a significant amount of battery chargers on a single tray within the Battery Control Electronics (BCE) stack, we built the rapid prototype units with a Printed Wiring Board (PWB) technology that had never been used in SS/L space flight technology before. Significant failures of more than one type occurred on the charger tray after relatively moderate levels of cumulative fatigue stress, demonstrating that this technology was not ready to move out of research and development into production. Development for this tray was stopped and redesigned using traditional PWB technology while the rest of the trays proceeded through additional HALT and qualification in parallel. Finding this issue early in the development process was significant and boosted the awareness of the validity of HALT at SS/L. The issue could have caused major cost and schedule issues if it had escaped our qualification program and been found at the satellite level. Had the issue occurred on orbit, the results for both SS/L and the customer could have been even more significant.

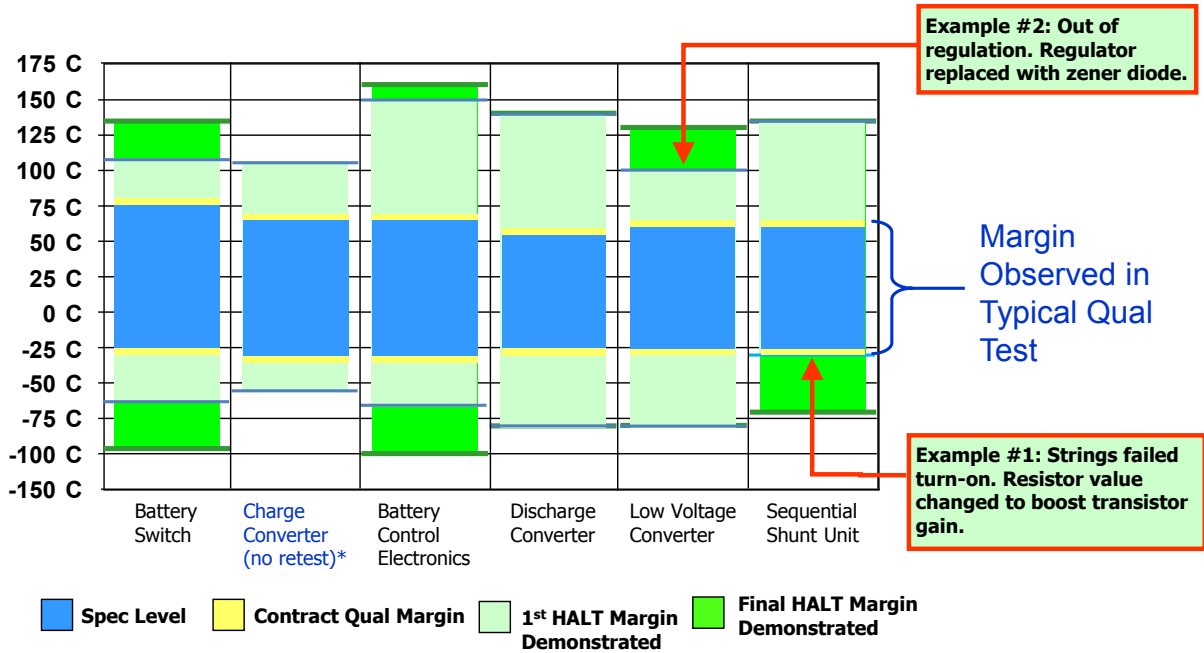
Table 2: SPS Unit and Tray Descriptions and HALT Decisions

Unit	Tray	HALT
Power Control Unit (PCU)	Discharge converter	Yes
	Error amplifier	Yes
	Sequential shunt	Yes
	Input/control	No
	Low-voltage converter	Yes
Battery Control Electronics (BCE)	Charger	Yes
	Battery command and telemetry	Yes
Battery Switch Tray (BST) (Part of Li-Ion battery assembly)		Yes

As an example of other findings during the HALT campaign, Figure 13 shows what was found during the hot and cold temperature step stress testing. The following observations are offered:

1. The most significant find during temperature testing was on the sequential shunt tray. See Example # 1 in Figure 11. At just a few degrees below the qualification temperature, some shunt strings failed to turn on. This is an excellent HALT example for the following reasons:
 - a. The fix (changing a resistor value to allow a transistor in the circuit to have more gain) was very easy and did not add any cost to the unit
 - b. The simple fix added 50 degrees C of operational margin to the unit. After the fix, the issue never manifested on the ground or in orbit in any of the 95 units built to date
 - c. Based on statistical distributions discussed previously, this problem most likely would have been found after production began and could have caused very expensive recalls and rework or on-orbit issues
2. Significant hot and cold temperature margins were demonstrated over MIL-SPEC-1540 calculated qualification levels during the first HALT on all of the other trays (the exception being the sequential shunt tray as discussed above)
3. The charge converter tray did not undergo a second temperature step HALT because of the redesign after the vibration testing discussed above. Even though the other trays showed significant operational margins during the first HALT, findings on four of the five other trays were deemed significant enough to fix. This is true for two of the five trays for both hot and cold margins. In all cases, the fixes were relatively easy, did not add significant cost or mass to the units, and resulted in more robust units as indicated by the additional margins shown during the second HALT (area shown in darker green)

4. One especially interesting finding was at the hot operational temperature margin demonstrated during the first HALT on the low-voltage converter. See Example # 2 in Figure 12. Although there was significant margin, the analysis of the limiting factor resulted in a design change that simplified and reduced the cost of the tray and added 25 degrees C of additional margin



*Note: New technology approach was scrapped after HALT vibration test anomalies

Figure 11: Li-ion SPS Electronics HALT Temperature Results

We are convinced that the success of this HALT campaign was instrumental in a successful qualification program and smooth transition into production. We are especially pleased with the on-orbit performance. As of June 30, 2012, 22 satellites, which have over 48 cumulative spacecraft years of operation, have been launched with the SPS, none of which have any performance limitation caused by any equipment that was part of the HALT campaign. On-orbit performance for the electronics that went through the HALT campaign is shown in Table 3.

Table 3: Super Power Subsystem On-orbit Performance

Unit	On-Orbit Op Time (CUM Hours)	# of Operating Units	Failed Units
Battery Switch Tray	1,328,586	69	0
Charge Converter	30,958,039	1,574	1
Battery Control Electronics	1,328,586	69	0
Discharge Converter	7,495,562	392	0
Low Voltage Converter	1,688,352	88	0
Error Amplifier Tray	484,929	31	0
Sequential Shunt Unit	1,633,449	95	0
TOTAL	44,917,502	2,318	1

SS/L MODIFICATIONS FROM TRADITIONAL HALT

Traditional HALT uses a step stress approach where progressively higher stress levels of one stimulus are applied until operational and destruct limits are found. If a destruct limit is manifested, the test article must be repaired before the testing can continue to the next stimulus in the test sequence. At SS/L, this process is often refined to emphasize searching for the operating limit margins for each stimulus first before purposely searching for any destruct limits. (Sometimes destruct limits, especially during vibration testing, are found whether you are trying to find them or not.) We have adopted this modification to the traditional HALT process because of the following:

- Limited number of test articles (satellite flight hardware is expensive)
- Product performance knowledge gained from our HALT history
- Product limitations identified during the DDQP review or HALT test readiness review
- Observed HALT schedule efficiency with this approach

Once all of the operating limit margins for each stimulus have been demonstrated, we can then purposely search for destruct limits by subjecting the test article to an extended combined environment test (see Figure 13). This is accomplished by adjusting the temperature set-points to incremental levels beyond the established operating testing limits, alternating between cold and hot steps. The vibration set-point can also be adjusted to the maximum established operating limit during the last five minutes of each temperature dwell, which adds additional cumulative fatigue stress.

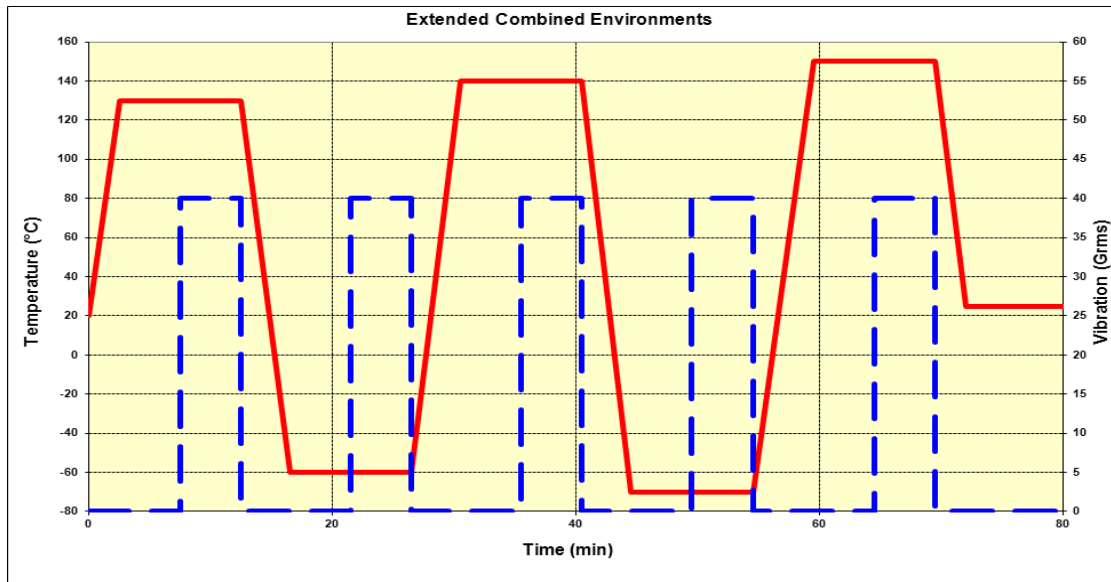


Figure 12: Extended Combined Environment Test

ADDITIONAL ADVANTAGES OF HALT

The main benefit of HALT, finding design limitations and fixing them to reduce the risk of problems after moving into production, has been discussed in many previously published papers. Hopefully this one has added to that collective knowledge. SS/L has observed other, perhaps less visible, but very important benefits of performing HALT:

- Improved responsible engineer knowledge of circuit operation. Troubleshooting anomalies manifested by HALT often result in interesting discoveries about circuit operation
- Improved test engineer knowledge of unit operation and test system functionality. When automated test equipment (ATE) can be made available for HALT, which is typically prior to when it would be needed for qualification testing, bugs can be worked out, thus increasing the test equipment fidelity prior to testing the qualification article
- Ability to convince customers that new technology is ready for insertion into flight programs
- Ability to convince insurance providers that new technology is ready for insertion into flight programs
- Convincing proof that there is a reason for material- and process-related design standards such as bonding, staking, proper solder pad sizes, etc. Although we always strive to have HALT articles representative of flight production models, to save cost and schedule they are often not built to the full flight production paper work and do not have Quality Control monitoring during production. HALT has an ability to find any nonflight material or process steps that may not have been disclosed at the test readiness review. This is a further validation of the effectiveness of HALT, plus it convinces employees of the importance of rigorous standards

- Additionally, there are uses for this equipment after the completion of HALT, such as new ATE check out, software development, retrofitting to test out parts obsolescence recovery, etc.

CONCLUSION

SS/L has validated over a 16-year period the value of performing HALT on new units intended for commercial satellite use. As indicated earlier, we do not perform HALT on everything. We use the DDQP to assess the risks associated with the amount and types of new technology being introduced, and determine when HALT is appropriate. Through this process, we have improved first-pass success during subsequent MIL-STD-1540 qualification testing, reduced the number of problems once in production, and improved our on-orbit performance. These results are vitally important to our profit bottom line, plus they improve customer and insurance provider confidence in our ability to introduce new technology successfully.

While writing this paper, SS/L achieved a significant milestone: HALT was completed on our next generation 15W DC/DC converter. Thus, the first development unit on which we performed HALT is nearing the end of its life cycle. Its on-orbit performance, 823 units with over 20 million hours of failure-free operation, speaks volumes for the robustness proven by HALT. Equally important is the culture developed at SS/L, as evidenced by the results of the HALT on the new 15W DC/DC converter: We experienced a failure during the last cycle of the combined environments (rapid temperature cycles with simultaneous vibration) test. The HALT Failure Review Team unanimously agreed to implement a design fix despite the fact that the failure didn't manifest until after 3 hours of extreme temperature step stresses, 20 temperature extreme cycles at a ramp rate of 25°C/minute, and over 460 minutes of cumulative vibration fatigue testing, which is well beyond the application stresses that the unit will be operated in. Everyone looked at the technical issue revealed by HALT and jointly determined that it should be fixed to add to the robustness of the unit and, thus, reduce the probability of a qualification, ground-based production test, or on-orbit failure. The fix did not increase the mass or cost of the unit, but the decision to improve it was in line with all four of SS/L's Core Values: Act With Integrity; Do It Right; Learn, Apply, Improve; Make the Company Stronger.

ACRONYMS/TERMS

ATE	Automated Test Equipment
DDQP	Design, Development, and Qualification Plan
Destruct limit	Unit ceases to function and does not resume normal operation until repairs are affected
HALT	Highly Accelerated Life Testing
Operational limit	Unit does not meet a performance parameter at some stimulus level, but comes back into specification after the stimulus level is reduced.
SPS	Super Power Subsystem
Stack or unit	Assembly of electronic trays into a functional stand-alone unit that get mounted to a panel at the satellite level; this is typically the level at which MIL-STD-1540 qualification and acceptance testing is performed.
Tray	Electronic circuitry mounted in a chassis, which may or may not have a cover prior to being integrated into a stack/unit; this is typically the level at which HALT is performed.

APPENDIX 1

HALT definitions obtained from “What is HALT? (and What Is *Not* HALT)” by Mile Silverman, CRE, Managing Partner Ops A La Carte. ASTR 2010 Oct 6- Oct 8, 2010 Denver CO

HALT: Done to ruggedize the product and obtain large margins over the expected in-use conditions. Uses all stresses which can cause relevant failures. Stresses are not limited to field levels or stresses.

— “Accelerated Reliability Engineering: HALT and HASS,” Gregg Hobbs

HALT: A method used to uncover design and process related flaws that would otherwise go undetected until the product is in the customer’s hands. It involves step stressing, rapid thermal transitions, and combined stressing of the product under various environmental conditions.

— “HALT, HASS, and HASA Explained,” Harry W. McLean- “HALT, HASS, and HASA Explained,” Harry W. McLean

HALT: An accelerated test designed to identify field failures before the first product is shipped. It is a method to apply stresses to a product while still in the design phase, which will reveal imperfections, design errors, and design marginality.

— “Improving Product Reliability: Strategies and Implementation,” Levin and Kalal

HALT: A stress testing methodology for accelerating product reliability during the engineering development process. It is commonly applied to electronic equipment and is performed to identify and thus help resolve design and is performed to identify and thus help resolve design weaknesses in newly-developed equipment

— Wikipedia

HALT: To quickly precipitate failures to identify and mitigate design weaknesses in a product in order to increase robustness during the product field use. This type of accelerated test is not intended to measure but to increase product reliability through the elimination of failure modes with the broadest separation between fieldstress and product strength. (Figures 1 a and b) This type of an accelerated test only identifies potential failure modes and guides the development and improvement processes for the chosen stressors.

— IEC Accelerated testing proposal_ Complete draft revC

HALT: Design test used to improve the robustness/reliability of a product through test-fail-fix process where applied stresses are beyond the specified operating limits.

— IPC-9592 “Performance Parameters for Power Conversion Devices”

HALT: A process specifically designed to find design weaknesses in products. It is not a pass/fail test, but a discovery test. The idea is to purposely stress products to the point of failure so that you can understand the mechanisms that are most likely to make them fail during their life cycle of transportation, storage, and use. The test assets overall life time is greatly compressed by means of the increased severity of the applied environmental stresses.

— IEST HALT Spec, Work in Progress

HALT: A design technique used to discover product weaknesses and design margins. The intent is to systematically subject a product to stress stimuli well beyond the expected field environments in order to determine the operating and destruct limits of your product.

— 50 Ways to Improve Your Product Reliability, Mike Silverman

BIOGRAPHY

Brian Kosinski is a veteran of 24 years government and commercial satellite industry experience. He has 20 years of increasing levels of responsibility at Space Systems/Loral (SS/L) and is currently the Executive Director of Product Reliability. In addition for being responsible for Reliability, Parts, Materials and Process disciplines; he has been instrumental in strengthening product development procedures and implementing robust qualification and failure review practices at SS/L.

Brian holds a bachelor's degree in Physics from the United States Naval Academy and a Master's degree in Electrical Engineering obtained from the Space Systems Engineering curriculum at the Naval Postgraduate School in Monterey California. He and his family live in Mountain View, California.

Dennis Cronin has been with SS/L for over 2 years working as a Product Development and Qualification Engineer managing its HALT programs. During this time, he has directed eight HALT tests that have identified key failure mechanisms and helped drive the root cause analyses to efficient and cost-effective corrective actions.

Prior to SS/L, Dennis spent over 20 years at Rockwell Collins, San Jose, California, where he led the successful completion of the first HALT test of the Joint Helmet-Mounted Cueing System (JHMCS) Helmet Mounted Display (HMD) which is currently used by the US military. He also managed reliability, accelerated life, durability and environmental qualification tests on various ruggedized military and commercial avionic displays and ground based systems.